17. (Amended) An information management system for semiconductor devices according to claim 16, wherein: said product ID information corresponds to chip ID information provided as a two-dimensional matrix code pattern for information management for each chip.

18. (Amended) A semiconductor device according to claim 16, wherein: said product ID information corresponds to frame ID information provided as a two-dimensional matrix code pattern for information management on a lead frame to which semiconductor chips are bonded.

~~21~~. A semiconductor device according to claim 1, wherein said two-dimensional matrix code pattern is formed on said semiconductor chip by photolithography.

REMARKS

The Office Action of June 4, 2001 and the references cited therein have been carefully considered.

In this Amendment the specification and claims have been amended to clarify the meaning of the term "two-dimensional barcode pattern" used in the present application, consistent with the description and definition of the "two-dimensional barcode pattern" as found on page 11 lines 1-17 of the present application as originally filed, without changing the intended scope of the claim and to avoid possible misunderstanding and ambiguity. More specifically, each of the independent claims has been amended to change the term "two-dimensional barcode pattern" to two-dimensional matrix pattern", and to positively state that the recited blocks forming the matrix code are "square blocks". It is submitted that these changes are consistent

with the arguments previously made and do not raise any new issues praising further search and or consideration. Accordingly, entry thereof is respectfully requested. The dependent claims have been amended so that they are consistent with the independent claims as amended.

Reconsideration of rejections of claims 1-21 under 35 U.S.C. 103(a) as being unpatentable over the Merlin et al. reference in view of the Shamir reference is respectfully requested. Since these references were discussed in the prior Amendments, and since those remarks concerning these references are still believed to be pertinent, they are incorporated herein by reference rather than repeating same. However, the following additional remarks are made in view of the above amendments.

As pointed out above, each of the independent claims has been amended to avoid the term "barcode" in order to more clearly distinguish the invention over that of the cited combination of references and in response to the Examiner's comments regarding duplication. As discussed in the Remarks contained in the last Amendment, it is submitted that the cited combination of references does not have any structure equivalent to the recited feature of the invention of a "two dimensional code pattern" of any type and in particular, a two-dimensional matrix code pattern comprised of a plurality of blocks, in particular square blocks, arranged in a two-dimensional matrix in a predetermined two dimensional region. Neither this feature nor the specific location of the specific type information is taught, suggested or made obvious by the cited combination of references.

In explaining this ground of rejection, the Examiner has taken the position that the reference numeral 1 in the Merlin et al. reference is equivalent to a semiconductor device and that the portions indicated by reference numerals 11, 12, and 13 constitute wafer surfaces. It is submitted that this assertion is inaccurate and not in keeping with the teachings of Merlin et al.

In the Merlin et al. reference, which relates to an IC module mounted on a card, the reference numeral 16 indicates a semiconductor chip and the reference numeral 1 indicates a substrate on which the IC module is mounted. Merlin et al. does not disclose that the wafer used to form a plurality of chips, and the reference numerals 11, 12 and 13 in Merlin et al. indicate external electrodes or the like provided on the IC module 10. In this regard, see Figures 1 and 2 and the description in Merlin et al. Unlike the present invention, Merlin et al. does not disclose or imply in any way whatsoever that a pattern should be provided on a chip, a lead frame or the like for any purpose whatsoever. In addition, Merlin et al. simply discloses that a mark 20 constituted of a plurality of alphanumerical characters is provided. In this reference, the pattern is provided on a different object from that to which the pattern is provided according to the present invention and, as recognized by the Examiner, Merlin et al. discloses a pattern which is formed in a completely different manner than a pattern according to the present invention.

In order to overcome this deficiency of the Merlin et al., the Examiner has cited the Shamir reference which simply discloses a conventional bar code pattern applied to a chip or housing. It is submitted, however, that since a code is not provided on a chip or lead frame in the Merlin et al. reference as is required according to independent claims of the present application, the technology of Shamir can not be directly combined with that of Merlin et al. as suggested by the Examiner. Moreover, and possibly more importantly, even if it were obvious to one skilled in the art to combine the teachings of the two references, the resulting combination would simply imply the use of a bar code as taught by Shamir or a code achieved by combining a bar code with numerals and characters, but would not in any way teach or render it obvious to provide a pattern to correspond to that recited in the claims of two-dimensional matrix code constituted by arranging a plurality of square blocks in two-dimensional directions. It is again pointed out that

this is not a mere duplication of a conventional barcode but an entirely different type of structural code arrangement. It should further be noted that if both a barcode and numerals or characters as suggested by the cited references are used in the code area, the code area will have to include the area to be occupied by the barcode and the area to be occupied by the characters or the numerals, and if the number of character or numerals have to be increased to provide additional coded information, the coding area is bound to become quite large as pointed out in the present application. Furthermore, when there are two different types of patterns, such as a barcode and characters or numerals in a code, complex controls must be implemented on the apparatus for providing these two types of patterns and two different means must be provided to read the code, which results in a more complex read operation since two different codes would have to be decoded to obtain the information. This is clearly undesirable.

The present invention overcomes these problems of two different types of codes by using a two-dimensional matrix code pattern constituted by arraying a plurality of square blocks in two-dimensional directions. By adopting such a code structure, the present invention addresses the problems of the cited references and those which would result from the combining the technologies disclosed in the cited references.

In summary, while the Examiner has asserted that a two-dimensional bar code pattern is an obvious duplication of a conventional one dimensional barcode, the application, as originally filed, defines a "two-dimensional" barcode in a specific manner, and the claims have now been amended to bring out this distinction. In particular, the term "two-dimensional bar code" has been deleted from the claims and replace by the term "two-dimensional matrix code". Moreover, each of the independent claims specifically recites that the matrix code is formed of an array of square blocks arranged in a two-dimensional matrix. Clearly, this is not a simple modification of

a conventional barcode as taught by Shamir, which features a simple one dimension or linear barcode pattern comprised of lines with different thickness and or spacings. It is therefore submitted that it is clear that the matrix code pattern disclosed and claimed according to the present invention is not obvious of a person skilled in the art from any of the cited references, so that each of claims 1-21 is allowable over the cited combination of the Merlin et al. and Shamir references under 35 U.S.C. 103.

In view of the above amendment, for the above stated reasons, it is submitted that all of the pending claims, i.e., claims 1-21 are allowable over the prior art of record, and are in condition for allowance. Such action in the passing of this application to issue therefore are respectfully requested.

A request for the necessary extension in the period for filing Amendment, as well as a check in payment of the applicable extension fee are attached.

If the Examiner's opinion that the prosecution of this application would be advanced by a personal interview, the Examiner is invited to telephone the undersigned counsel to arrange for such an interview.

Respectfully submitted,

Norman N. Kunitz
(Registration No. 20,586)
VENABLE
Post Office Box 34385
Washington, DC 20043-9998
Telephone: (202) 962-4800
Telefax : (202) 962-8300

NNK:srb dlw
DC2 322304

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

The paragraph on page 3, spanning lines 12-26 have been amended as follows:

Alternatively, since a read operation can be performed with ease by employing an optical apparatus, various types of information are recorded by utilizing one-dimensional [bar]code patterns in the inter-process physical distribution of semiconductor devices in some semiconductor manufacturing methods. However, there is a limit to the quantity of information that can be recorded in a one-dimensional [bar]code pattern per unit area, and since the area occupied by the one-dimensional [bar]code pattern must increase for a larger quantity of information to be carried, information management using one-dimensional [bar]code patterns will not always be sufficient in a semiconductor devices with only limited space available for recording information are handled.

The paragraphs on page 5, spanning line 12 to page 6 line 10 have been amended as follows:

In order to achieve the objects stated above, in a first aspect of the present invention, a semiconductor device is provided that is characterized in that a two-dimensional [bar]code or matrix code pattern for information management is projected and exposed as chip ID information on each of the chips arrayed on the wafer surface. It is to be noted that since chip ID information is provided in the two-dimensional [bar]code pattern, it becomes possible to make use of chip information that is inherent to each chip.

Since the quantity of information that can be recorded per unit area of a two-dimensional [bar]code pattern is very large and recognition utilizing an optical apparatus can be implemented

with ease, marking can be made on each of the chips arrayed on the wafer surface, which has not been possible in the prior art, so the information management can be easily implemented for chips on an individual basis.

In addition, as a method for marking a two-dimensional [bar]code pattern on each chip, projection and exposure may be implemented by employing a liquid crystal mask capable of changing transmitted patterns for different exposures to provide different chip ID information for each wafer using the same mask.

In order to achieve the objects described above, in a second aspect of the present invention, a semiconductor device is provided that is characterized in that marking is implemented with two-dimensional [bar]code patterns for information management as framed ID information on lead frames to which semiconductor chips are bonded. It is to be noted that in the frame ID information in the two-dimensional [bar]code pattern, chip positional information indicating the position of chips within the frame and the chip ID information may be included.

The paragraph on page 6 spanning lines 18-30 have been amended as follows:

In order to achieve the objects described above, in a third aspect of the presentation, a semiconductor device that is characterized in that marking for information management is implemented with a two-dimensional [bar]code pattern as product ID information on the outer surface of a package of resin-sealed semiconductor chips. It is to be notes that in the product ID information recorded in the two-dimensional [bar]code, additional information and chip ID information corresponding to each of the resin-sealed chips can be included. With this structure, even in a state in which chips cannot be visually checked after molding, information management can be implemented for each chip.

The paragraph on page 7 spanning line 29 to page 8 line 2 have been amended as follows:

As explained above, by using the chip ID information, the frame ID information and the product ID information that are coded through two-dimensional [bar]code patterns in the inter-process physical distribution during the semiconductor manufacturing processes, detailed management can be implemented for individual chips, thereby making it possible to establish a semiconductor manufacturing facility that is capable of supporting production of many different types of products in small quantities with a high degree of flexibility.

The paragraph on page 8 spanning lines 20-22 have been amended as follows:

FIG. 1 illustrates a schematic structure of an embodiment of a two-dimensional [bar] matrix code that may be adopted in the present invention;

The paragraph on page 8 spanning lines 25-27 have been amended as follows:

FIG.3 illustrated an embodiment of a two-dimensional [bar] matrix code pattern forward on a semiconductor chip according to the present invention;

The paragraph on page 8 spanning lines 28-31 have been amended as follows:

FIG. 4 illustrated an embodiment of the liquid crystal mask employed to project and expose a two-dimensional [bar] matrix code pattern on a semiconductor chip according to the present invention;

The paragraph on page 9 spanning lines 16-20 have been amended as follows:

FIG. 10 is a block diagram illustrating the schematic structure of a die bonder that is capable of adding a two-dimensional; [bar] matrix code pattern to a lead time during the bonding step according to the present invention;

The paragraph on page 10 spanning lines 7-9 have been amended as follows:

FIG. 17 illustrates a state in which character information and a two-dimensional [bar] matrix code pattern are printed at the package;

The paragraph on page 10 spanning line 33 to page 11 line 17 have been amended as follows:

First, in FIG. 1, an example of a two-dimensional barcode or matrix code pattern which may be employed in an embodiment of the present invention is shown. As shown in the figure, a two-dimensional barcode or matrix code pattern 10 is a two-dimensional pattern in which specific information can be recorded by coloring the squares 11 of a grid in black or white to form blocks that extends two-dimensionally in conformance to predetermined rules. It is to be noted that while the encoding rules for coloring the grid black and white in the two-dimensional pattern may be the same as those in the prior art, new encoding rules may be created instead. A detailed explanation of the actual method for coloring the grid black and white is omitted since it does not bear direct relevance to the contents of the present invention. However, since data error detection can be encoded as part of the encoding rules, and in that case, errors when reading two-dimensional barcode patterns recorded at individual chips, individual frames and individual resin-sealed semiconductor chips can be reduced, as detailed later.

The paragraph on page 12 spanning line 4-9 have been amended as follows:

In contrast, the inventor of the present invention has observed that the two-dimensional barcode or matrix code pattern adopted in the present invention provides the following superior features compared to the character information patterns and one-dimensional barcode patterns in the prior art.

The paragraphs on page 12 spanning line 29 to page 13 line 5 have been amended as follows:

The inventor of the present invention has conducted focused research into the features of the two-dimensional [bar]code patterns described above, which has cumulated the completion of the present invention, which achieves efficient and accurate information management in the inter-process physical distribution in the semiconductor manufacturing processes by utilizing two-dimensional [bar]code patterns at various stages in the semiconductor manufacturing processes.

The following is a detailed explanation of embodiments in which two-dimensional barcode i.e., matrix codes according to the invention are used at various stages in the semiconductor manufacturing processes.

The paragraphs on page 13 spanning line 7 to page 14 line 31 have been amended as follows:

In this embodiment, in the wafer process, two-dimensional [bar]code patterns 30 as chip ID information, i.e., two-dimensional [bar]code patterns 30-1, 30-2 and 30-3, are recorded at

specific positions (lower left positions in the figure, for instance) of individual chips 31-1, 31-2, and 31-3 respectively formed in each wafer, as shown in FIG. 3. The chip ID information may be recorded during the photolithography step for wiring that is implemented near the end of the wafer process, for instance, by projecting and exposing the two-dimensional [bar]code pattern corresponding to the chip ID information at the specific position of each chip during projection and exposure.

FIG. 4 shows an embodiment of the liquid crystal mask that is employed to project and expose the chip ID information on each chip. This liquid crystal mask 40 is capable of changing the liquid crystal arrangement of the individual grid squares to render a light-transmitting light-blocking pattern corresponding to the two-dimensional [bar]code pattern on the mask surface. In a chip ID generating unit 41, chip ID information such as the product name, the lot ID and the chip positional coordinates for each chip is obtained. In a two-dimensional [bar]code conversion unit 42, the chip ID information transmitted from the chip ID generating unit 41 is converted to a two-dimensional [bar]code pattern. A liquid crystal driver 43 changes the light transmitting light blocking pattern in the individual grids formed by the liquid crystal mask 40 as appropriate, and the light transmitting light blocking pattern which is converted to a two-dimensional [bar]code pattern at the two-dimensional [bar]code conversion unit 42 is rendered on the liquid crystal mask 40 by the liquid crystal driver 43.

Then, by using this liquid crystal mask 40, exposure is performed at a specific position on each chip with a projection exposure apparatus (not shown) to develop a two-dimensional [bar]code pattern inherent to each chip. After this, by implementing the photolithography step and the etching step as in normal processing, a two-dimensional [bar]code pattern inherent to each chip is formed. It is to be noted that while an example in which different two-dimensional

[bar]code patterns are provided for the individual chips is presented above, it foes without saying that a singles two-dimensional [bar]code pattern can be formed for all the chips.

As has been explained, in this embodiment, it is possible to add chip ID information for distinguishing the individual chips in a wafer from one another while taking up an extremely small area on the individual chips of the wafer, and thus, individual chips on a wafer surface can be distinguished from one another, which is not possible in the prior art. In addition, by forming two-dimensional [bar]code patterns on chips during the wiring step in the wafer process, chip ID information can be recorded for each chip without having to allocate special space for accommodating the two-dimensional [bar]code pattern. Furthermore, by utilizing the liquid crystal mask 40 shown in FIG. 4, chip ID information that is different for each chip can be recorded using one mask.

IN THE CLAIMS:

The following claims have been amended as follows:

1. (Four Times Amended) A semiconductor device having at least one semiconductor chip manufactured from a wafer, said semiconductor chip comprising said device and having a two-dimensional [barcode] matrix code pattern for information management provided on a surface of said at least one semiconductor chip with the pattern representing chip ID information, and said two-dimensional [barcode] matrix code pattern is comprised of a plurality of square blocks arranged in a matrix in a predetermined two-dimensional region.

4. (Thrice Amended) A semiconductor device manufactured using a lead frame, with the lead frame having a two-dimensional [barcode] matrix code pattern for information management provided on said lead frame to which semiconductor ships are bonded, with the pattern representing frame ID information, and said two-dimensional [barcode] matrix code pattern is comprised of a plurality of square blocks arranged in a predetermined two-dimensional region.

6. (Amended) A semiconductor device according to claim 4, wherein: said frame ID information is made to correspond to chip ID information provided as a two-dimensional [barcode] matrix code pattern for information management for each chip.

7. (Twice Amended) A semiconductor device having at least one semiconductor ship sealed by resin, and having a two-dimensional [barcode] matrix code pattern for information management provided at an outer surface of said resin and representing product ID information, and said two-dimensional [barcode] matrix code pattern is comprised of a plurality of square blocks arranged in a matrix in a predetermined two-dimensional region.

9. (Amended) A semiconductor device according to claim 7, wherein: said product ID information corresponds to chip ID information provided as a two-dimensional [barcode] matrix code pattern for information management for each chip.

10. (Amended) A semiconductor device according to claim 7, wherein: said product ID information corresponds to frame ID information provided as a two-dimensional

[barcode] matrix code pattern for information management on a lead frame to which semiconductor chips are bonded.

11. (Thrice Amended) An information management system for semiconductor devices, having at least one semiconductor chip that implements management of information related to said semiconductor devices separately for individual semiconductor devices comprising:

a read device that reads ship ID information, said chip ID information is providcd on said semiconductor chip as a two-dimensional [barcode] matrix code pattern for information management for each chip, said two-dimensional [barcode] matrix code pattern is comprised of a plurality of square blocks arranged in a matrix in a predetermined two-dimensional region; and

a management unit that registers said chip ID information thus read and manages individual semiconductor manufacturing processes based upon said chip ID information thus registered.

14. (Thrice Amended) An information management system for semiconductor device manufactured using a lead frame, which system implements management of information related to said semiconductor devices separately for individual semiconductor devices comprising:

a read device that reads frame ID information, said frame ID information is provided on said lead frame as a two-dimensional [barcode] matrix pattern for information management, said two-dimensional [barcode] matrix code pattern is comprised of a plurality of square blocks arranged in a matrix in a predetermined two-dimensional region; and

a management unit that registers said frame ID information thus read and manages individual semiconductor manufacturing processes based upon said frame ID information thus registered.

16. (Thrice Amended) An information management system for semiconductor devices having semiconductor chips sealed by resin, which system implements management of information related to said semiconductor devices separately for individual semiconductor devices comprising:

a read device that reads product ID information, said product ID information is provided as a two-dimensional [barcode] matrix pattern for information management at an outer surface of said resin, said two-dimensional [barcode] matrix pattern is comprised of a plurality of square blocks arranged in a matrix in a predetermined two-dimensional region; and

a management unit that registers said product ID information thus read and manages a product shipping process based upon said product ID information thus registered.

17. (Amended) An information management system for semiconductor devices according to claim 16, wherein: said product ID information corresponds to chip ID information provided as a two-dimensional [barcode] matrix code pattern for information management for each chip.

18. (Amended) A semiconductor device according to claim 16, wherein: said product ID information corresponds to frame ID information provided as a two-dimensional

[barcode] matrix code pattern for information management on a lead frame to which semiconductor chips are bonded.

21. A semiconductor device according to claim 1, wherein said two-dimensional [barcode] matrix code pattern is [as] formed on said semiconductor chip by photolithography.